ABSTRACT OF THE DISCLOSURE

A microcontroller device in which complex processing procedures to be executed iteratively are implemented in a hardware manner by finite state machines, the deice including a module for managing the processing procedures and an interrupt managing module, and a set of registers for enabling interruption of execution in the module, for managing the processing procedures and transfer of control to the interrupt manager, as well as for enabling restoration of the control to the manager of the processing procedures. The registers store information regarding the type of interrupt and the state on which it intervenes. Selection information is derived from the contents of the registers to establish whether the interrupt operates on a standard instruction or else on an iterative procedure, and in order to command operation of the control unit accordingly.